

10/8/03

PTO/SB/08A (08-03)

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## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

**(Use as many sheets as necessary)**

Sheet 1

of 1

<b>Complete if Known</b>	
Application Number	10/681,525
Filing Date	10/8/2003
First Named Inventor	Srinivasan, Varadarajan
Art Unit	2827
Examiner Name	G. NV. Auduong
Attorney Docket Number	NLMI.P133

**U. S. PATENT DOCUMENTS**

## FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear
					T <sup>6</sup>

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**STATEMENT BY ATTENDEE**  
*(Use as many sheets as necessary)*

Sheet 1

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Application Number	10/681,525
Filing Date	October 8, 2003
First Named Inventor	Srinivasan, Varadarajan
Art Unit	2827
Examiner Name	G. N. Auduong
Attorney Docket Number	NLMI.P133

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Sheet

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Application Number	10/681,525
Filing Date	10/8/2003
First Named Inventor	Srinivasan, V.
Art Unit	2818 2827
Examiner Name	
Attorney Docket Number	
NLMI.P133	

### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
(L)		SAKURAI, T. et al., "A Low Power 46ns 256k bit CMOS Static RAM with Dynamic Double Word Line," IEEE Journal of Solid State Circuits, Vol. SC-19, No.5, October 1984, pp.578-585	
		SOOD, L. et al., "A Fast 8ki x 8 CMOS SRAM With Internal Power Down Design Techniques," IEEE Journal of Solid State Circuits, Vol. SC-20, No. 5, October 1985, pp.941-950	
		MIYAJI, F. et al., "A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads, IEEE Journal of Solid state Circuits," Vol. 24, No. 5, October 1989, pp.1213-1218	
		SASAKI, K. et al., " A 7-ns 140mW 1-Mb CMOS SRAM with Current Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1511-1518	
(L)		PRINCE, B., "Semiconductor Memories: A Handbook of Design, Manufacture and Application," 2nd Ed., John Wiley & Sons Ltd., West Sussex, England, 1995, pp. v-xvii, 401-404 and 4	

Examiner Signature	<i>See Subway</i>	Date Considered	4/05
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